MAP3514D

1-CH Quasi-Resonant Mode Buck Controller for LED Backlight

General Description

MAP3514D is a 1 channel quasi-resonant mode buck controller for LED backlight application. It operates at boundary conduction mode which provides better efficiency and lower EMI.

MAP3514D features ±2% current sensing (CS) voltage accuracy and has dedicated analog dimming input up to 3.3V. It can be powered from 8.5V ~ 18V supply.

MAP3514D provides MOSFET drain-source short detection for fault output, V_{CC} over voltage protection (OVP) for fault output, V_{CC} under voltage lockout (UVLO), Input voltage OVP detection, Input voltage UVP, current sense resistor short protection, short circuit protection (SCP) and standby mode.

MAP3514D is available 14 leads SOP with Halogen-free (fully RoHS compliant).

RoHS Compliant
HALOGEN-FREE

Features

- 8.5V to 18V Input Voltage Range
- Quasi-Resonant Mode
- LED Current Compensation Function
- Direct PWM Dimming Input
- ±2% Current Sensing Voltage Accuracy
- Fault Output (FLT pin)
  - MOSFET Drain-Source Short Detection
  - V_{CC} Over Voltage Protection Detection
- Short Circuit Protection
- Current Sense Resistor Short Protection
- V_{CC} Under Voltage Lock Out
- Input Voltage Under Voltage Protection Detection
- Input Voltage Over Voltage Protection Detection
- Standby Mode
- 14 Leads SOIC Package with Halogen-free

Applications

- High Brightness white LED backlighting for LCD TVs
- General LED lighting applications

Ordering Information

Part Number	Top Marking	Ambient Temperature Range	Package	RoHS Status
MAP3514DSIRH	MAP3514D	-40℃ to +85℃	14Leads SOIC	Halogen Free

Typical Application

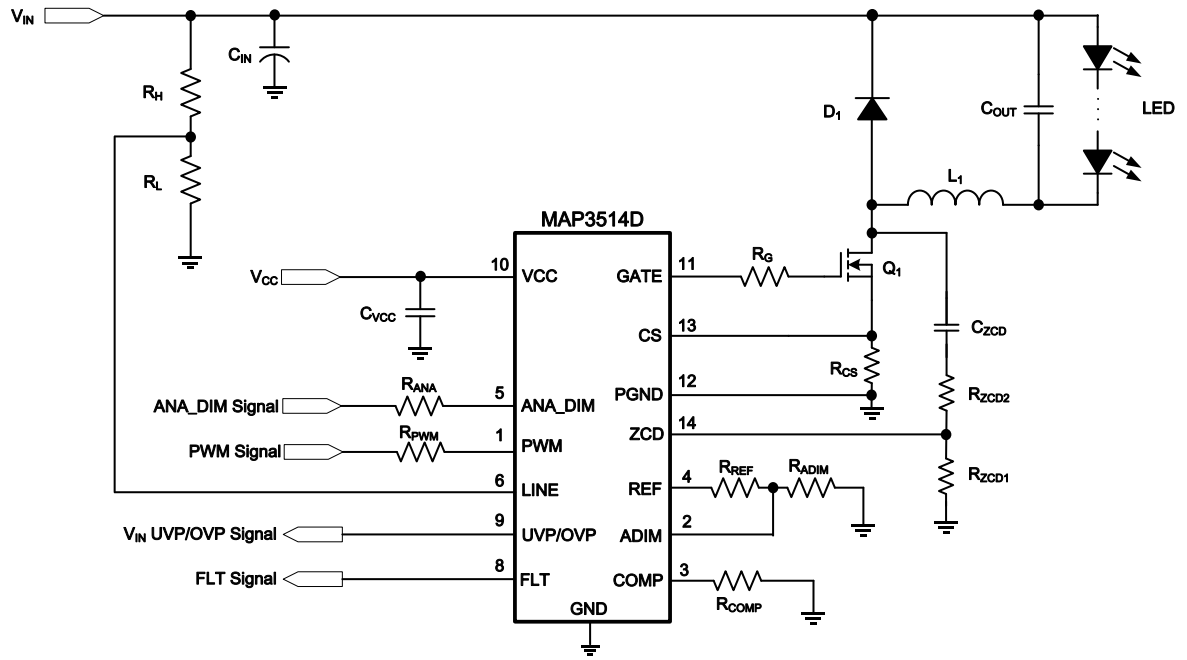


Figure 1. Quasi-resonant mode buck converter

Pin Configuration and Description

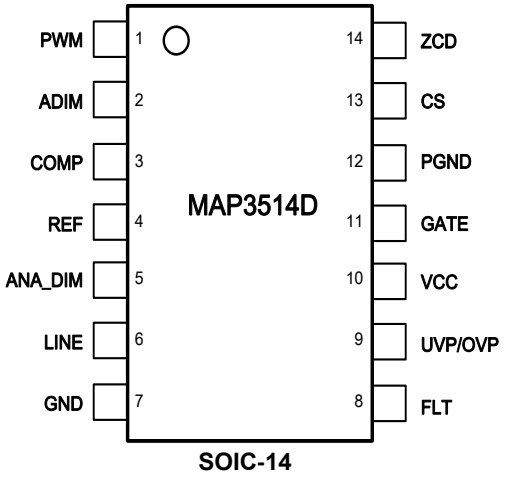


Figure 2. Pin Configuration (Top View)

Pin	Name	Description
1	PWM	PWM Dimming
2	ADIM	Internal Analog Dimming
3	COMP	LED Current Accuracy Compensation
4	REF	ADIM Buffer Output
5	ANA_DIM	External Analog Dimming Input
6	LINE	Input Voltage Detection (Note 1)
7	GND	Ground
8	FLT	Fault Output
9	UVP/OVP	Input Voltage UVP/OVP Signal Output
10	VCC	Power Supply Input
11	GATE	GATE Drive Output
12	PGND	Power Ground (Note 2)
13	CS	Current Sense
14	ZCD	Zero Current Detection

Note 1: Connect external resistor to LINE to detect the input voltage V_{IN} as shown in typical application
Note 2: Connect external resistor to PGND to sense the external power MOSFET source current as shown in typical application

Functional Block Diagram

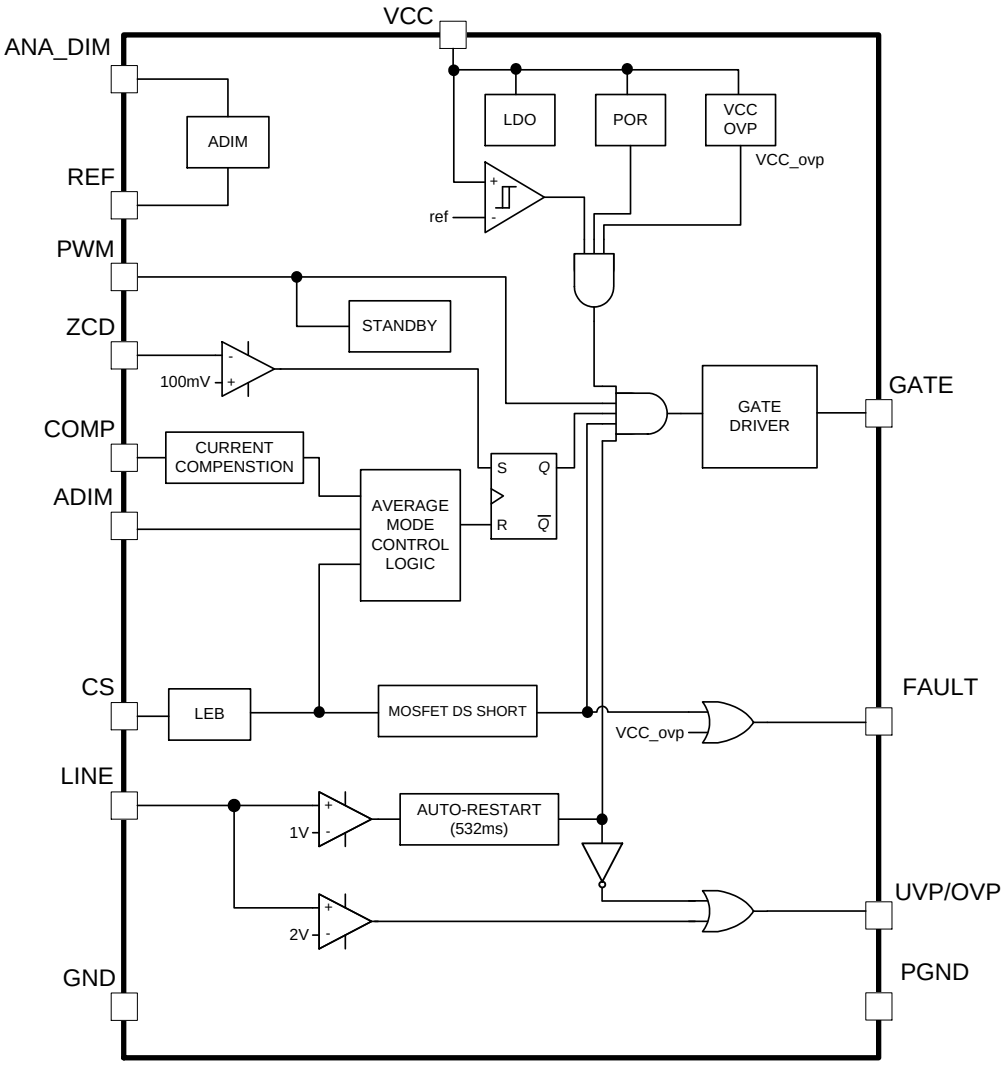


Figure 3. Block Diagram

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{CC}, V_{GATE}, V_{PWM}, V_{FLT}	VCC, GATE, PWM, FLT pins Voltage	-0.3	20	V
V_{ZCD}	ZCD pin Voltage	-0.7	20	V
V_{CS}, V_{REF}, V_{ADIM}, V_{ANA_DIM} V_{COMP}, V_{LINE}, $V_{UVP/OVP}$	CS, REF, ADIM, ANA_DIM, COMP, LINE, UVP/OVP pins Voltage	-0.3	5	V
T_{PAD}	Soldering Lead/ Pad Temperature 10sec		300	°C
T_J	Junction Temperature	-40	+150	°C
T_S	Storage Temperature	-65	+150	°C
ESD	HBM on All Pins (Note 2)	-2000	+2000	V
	MM on All Pins (Note 3)	-200	+200	
	CDM on All Pins (Note 4)	-500	+500	

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22A-114.
Note 3: ESD tested per JESD22A-115.
Note 4: ESD tested per JESD22C-101.

Recommended Operating Conditions (Note 1)

Parameter		Min	Max	Unit
V_{cc}	Supply Input Voltage	8.5	15(note2)	V
V_{ANA_DIM}	ANA_DIM Input Range	0.0	3.3	V
T_A	Ambient Temperature (Note 3)	-40	+85	°C

Note 1: Normal operation of the device is not guaranteed if operating the device over outside range of recommended conditions.
Note 2: If the supply input voltage (V_{CC}) exceeds typ.16V, the gate signal is shut down by the V_{CC} OVP function.
Note 3: The ambient temperature may have to be derated if used in high power dissipation and poor thermal resistance conditions.

Package Thermal Resistance (Note 1)

Parameter		$R_{\theta JA}$	$R_{\theta JC}$	Unit
MAP3514DSIRH	14 Leads SOIC	76.9	33.2	°C/W

Note 1: Multi-layer PCB based on JEDEC standard (JESD51-7)

Electrical Characteristics

Unless noted, V_{CC} = 12V, C_{VCC} = 1.0μF, and typical values are tested at T_A = 25°C.

Parameter		Test Condition	Min	Typ	Max	Unit
Supply						
V_{CC}	Input Voltage Range		8.5		18	V
I_Q	Quiescent Current	V_{PWM} = 0V, V_{CC} = 12V		2.0		mA
$I_{STANDBY}$	Standby Current	V_{CC} = 12V			600	uA
V_{CC_UVLO}	Under Voltage Lockout Threshold Voltage on VCC pin	Release threshold(rising V_{CC})	7.5	8.0	8.5	V
		Lockout hysteresis(falling V_{CC})	0.5	1.0	1.5	
t_{PG_DELAY}	Power Good Delay Time			500		ms
Zero-Current Sense						
V_{ZCDTH_FALL}	ZCD Threshold Voltage	Falling V_{ZCD}		100		mV
V_{ZCDTH_RISE}		Rising V_{ZCD}		200		mV
V_{ZCDHYS}	ZCD Hysteresis			100		mV
$t_{ZCDTOUT}$	ZCD Time-Out			25		us
GATE Driver						
I_{SOURCE}	GATE Source Current	V_{GATE} = 0V		300		mA
I_{SINK}	GATE Sink Current	V_{GATE} = V_{CC}=12V		600		mA
t_{RISE}	GATE Output Rising Time	C_{GATE} = 1nF, V_{CC} = 12V		70	150	ns
t_{FALL}	GATE Output Falling Time	C_{GATE} = 1nF, V_{CC} = 12V		35	100	ns
t_{ON_MAX}	Max. On-Time			13		us
f_{MAX}	Max. Frequency			1000		kHz
Current Sense & Dimming						
V_{ADIM}	ADIM Input Voltage Range		0.66		1.65	V
V_{CS}	CS Detection Voltage	V_{ADIM} = 0.66V		0.33		V
		V_{ADIM} = 1.65V		0.825		V
t_{LEB}	Leading Edge Blanking Time	(Note1)		350		ns
REF						
V_{ANA_DIM}	ANA_DIM Input Voltage Range		0		3.3	V
V_{REF}	REF Voltage	ANA_DIM = 0V		1.32		V
		ANA_DIM = 3.3V		3.3		V
		ANA_DIM > 3.6V		3.3		V
		ANA_DIM = open		3.3		V
COMP						
V_{COMP}	COMP Voltage			2		V
Logic Interface						
V_{PWM}	Logic Input Level on PWM pin	V_{PWM_L} : Logic Low			0.8	V
		V_{PWM_H} : Logic High	2.2			
R_{PWM}	Pull-down Resistor on PWM pin	V_{PWM} = 4V	50	100	150	kΩ

Note 1: These parameters, although guaranteed by design, are not tested in mass production.

Electrical Characteristics

Unless noted, V_{CC} = 12V, C_{VCC} = 1.0μF, and typical values are tested at T_A = 25°C.

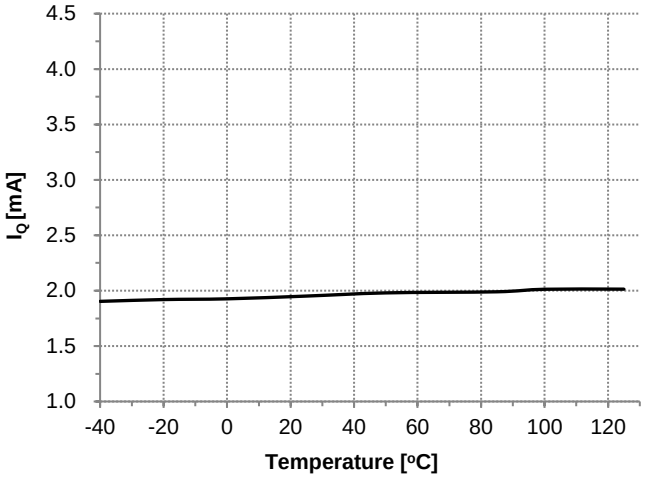
Parameter		Test Condition	Min	Typ	Max	Unit
Protection						
V_{SCP}	SCP Detection Threshold Voltage on CS pins		2.3	2.5	2.7	V
t_{DELAY}	SCP Delay Time			300		ns
$t_{RESTART}$	Restart Time			1		ms
V_{CSP}	RCS Short Detection Threshold Voltage on CS pin		0.15	0.2	0.25	V
t_{CSP}	RCS Short Detection Time			5		us
V_{SCPDS}	MOSFET DS Short Detection Threshold Voltage on CS pin	V_{PWM} = 3.3V	2.3	2.5	2.7	V
		V_{PWM} = 0V	0.5	0.7	0.9	V
t_{SCPDS}	MOSFET DS Short Detection Time			5		us
R_{FLT}	FLT pin Internal Resistance	I_{FLT} = 1mA	250	500	1000	Ω
V_{OVP_VCC}	V_{CC} OVP Detection threshold voltage			16		V
V_{CC_OVPHYS}	V_{CC} OVP Hysteresis			1		V
V_{UVP_LINE}	LINE UVP Detection threshold voltage		0.9	1	1.1	V
t_{UVP_LINE}	LINE UVP Detection Time			1.5		us
V_{OVP_LINE}	LINE OVP Detection threshold voltage		1.9	2	2.1	V
V_{LINE_HYS}	LINE Hysteresis			100		mV
$T_{SHUTDOWN}$	Thermal Shutdown Temperature			150		°C

Note 1: These parameters, although guaranteed by design, are not tested in mass production.

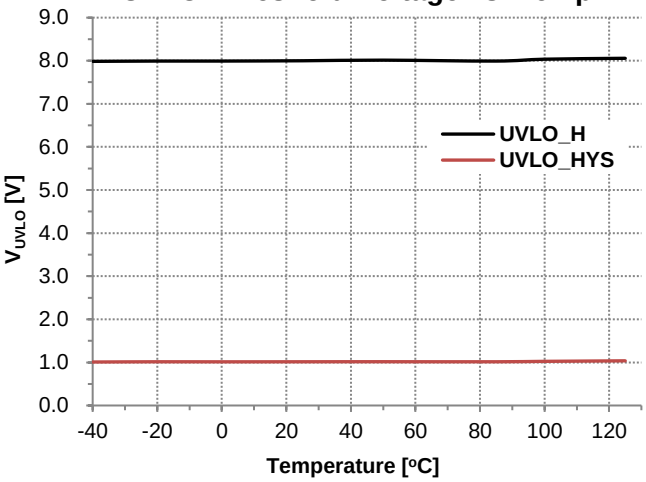
Typical Operating Characteristics

Unless otherwise noted, V_{CC} = 12V and T_A = 25°C.

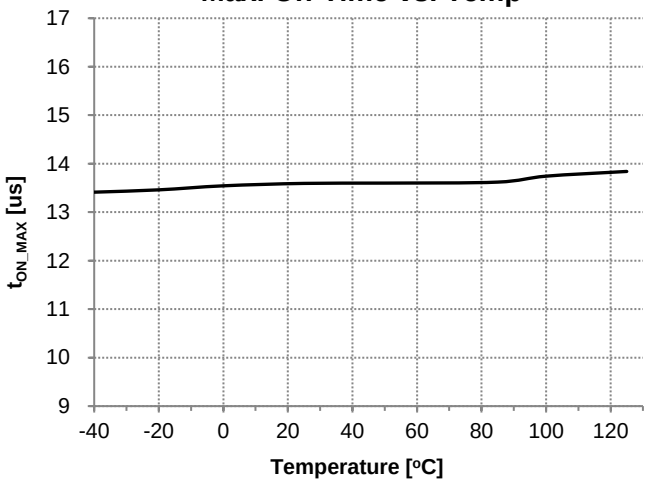
Quiescent Current vs. Temp



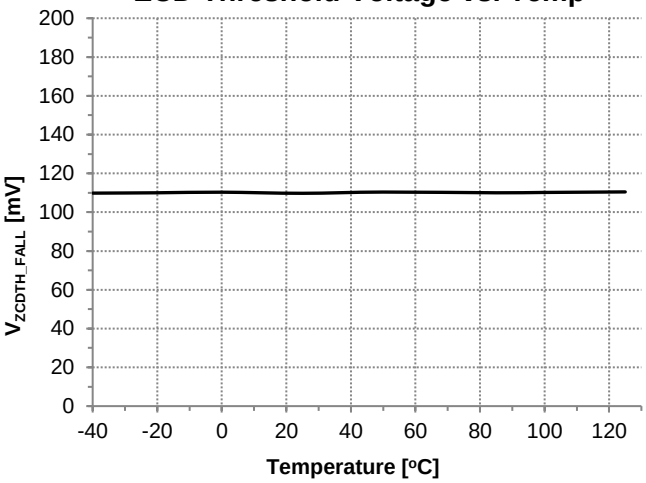
UVLO Threshold Voltage vs. Temp



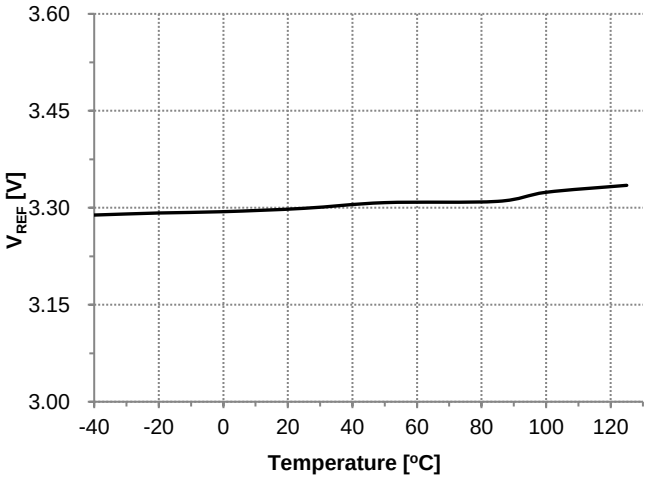
Max. On-Time vs. Temp



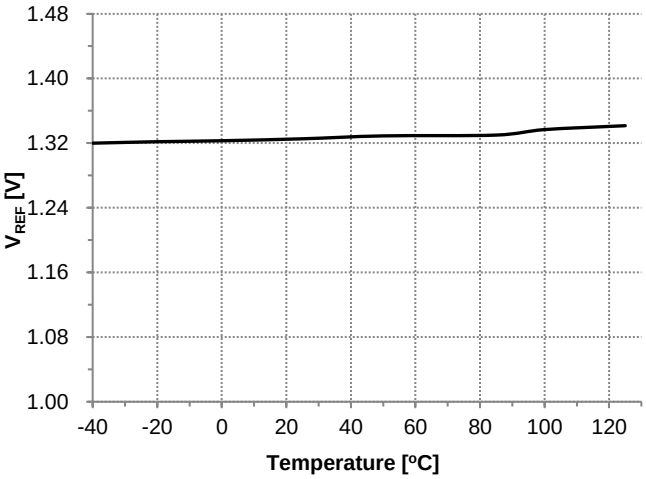
ZCD Threshold Voltage vs. Temp



REF Voltage vs. Temp (ANA_DIM=3.3V)



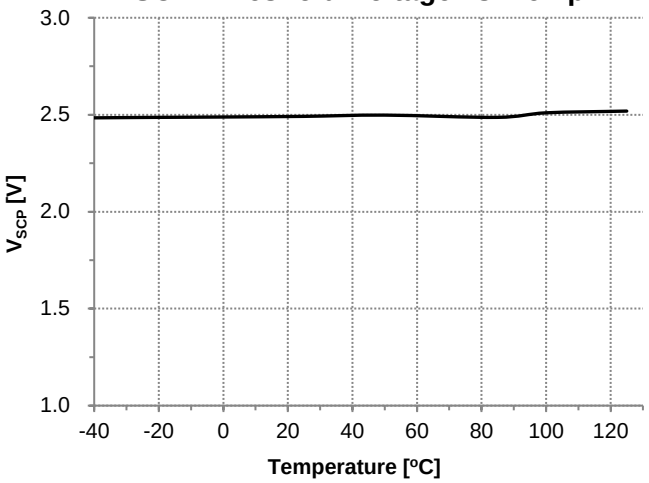
REF Voltage vs. Temp (ANA_DIM=0V)



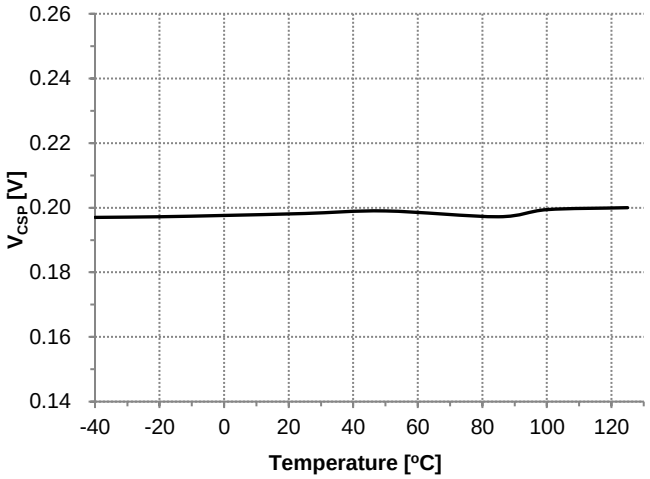
Typical Operating Characteristics

Unless otherwise noted, V_{CC} = 12V and T_A = 25°C.

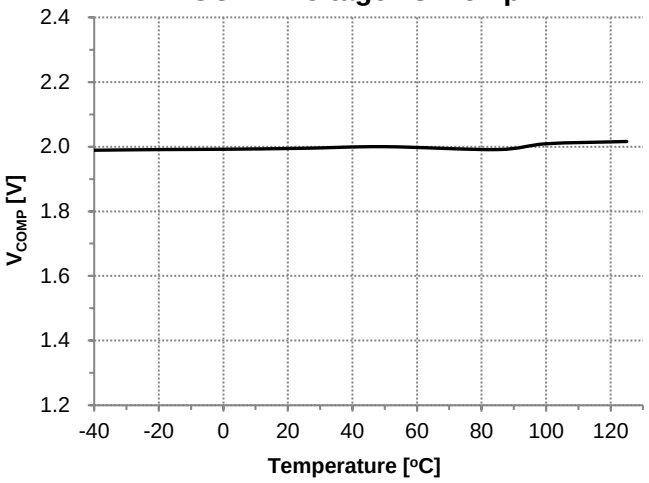
SCP Threshold Voltage vs. Temp



RCS Short Threshold Voltage vs. Temp



COMP Voltage vs. Temp



Functional Description

GENERAL DESCRIPTION

The MAP3514D is a low-side single switch buck controller optimized to LED backlight applications. It does not require any external loop compensation or high side current sensing.

The IC operates at boundary conduction mode which provides better efficiency and lower EMI.

LED CURRENT

The LED current is calculated by following equation.

$$I_{LED} = \frac{0.5V_{ADIM}}{R_{CS}}$$

$$= \frac{0.5 \times (0.66 + 0.3 \times V_{ANA\_DIM})}{R_{CS}} \text{ [A]} \quad (1)$$

When $R_{REF} = R_{ADIM}$.

The ANA_DIM voltage range is from 0.0V to 3.3V. The LED current changes according to ANA_DIM and ADIM.

In terms of total system accuracy of LED current, the larger inductance, the slower switching frequency and the larger minimum on time than 800ns, the better accuracy.

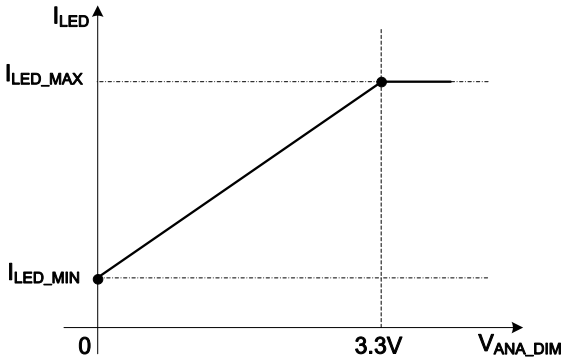


Figure 4. I_{LED} vs. V_{ANA_DIM} graph

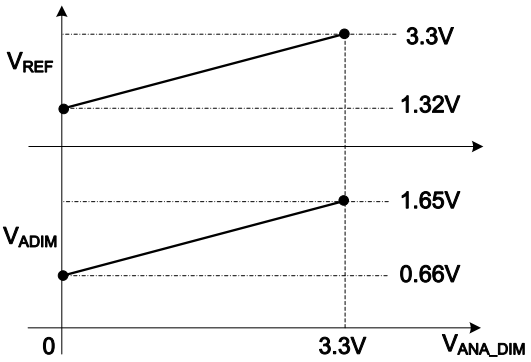


Figure 5. V_{REF} and V_{ADIM} vs. V_{ANA_DIM} graph (When $R_{REF} = R_{ADIM}$)

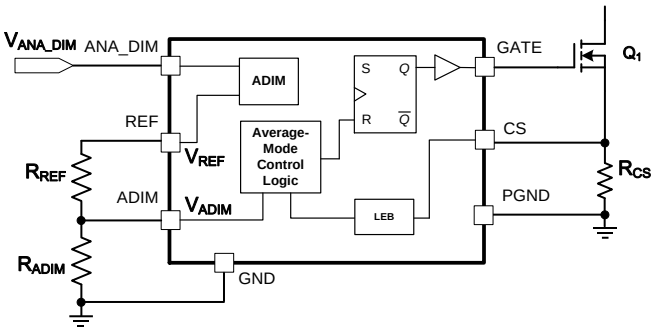


Figure 6. Configuration of analog dimming and current sensing

LED CURRENT COMPENSATION

MAP3514D has the LED current compensation function by using COMP pin.

LED current offset can be occurred by the input/output condition and the components of the buck converter.

The compensation resistor R_{COMP} is used to control the offset voltage of ADIM. The COMP voltage is typ. 2V and the compensation current I_{COMP} is fixed by R_{COMP}.

By Internal current compensation circuit, 1/n times I_{COMP} current flows to ADIM pin. By this current, the offset voltage of ADIM is generated. Consequently, LED current is compensated by R_{COMP}.

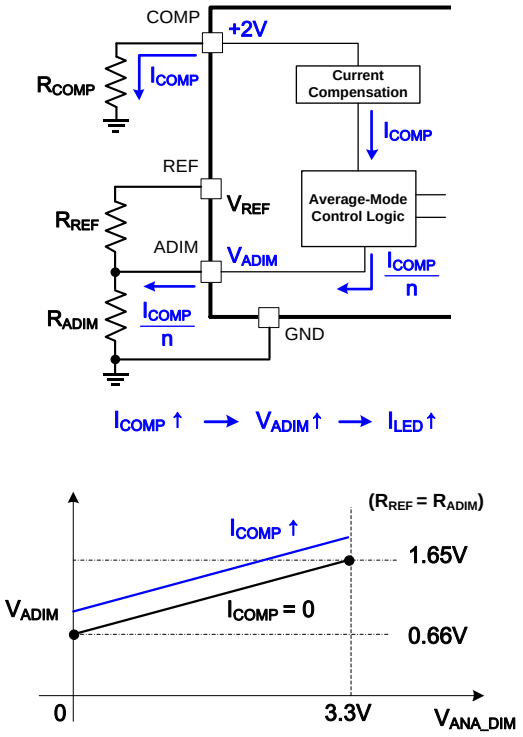


Figure 7. Configuration of LED current compensation

ZERO-CURRENT SENSE

The MAP3514D is a boundary conduction mode (BCM) buck controller operating at resonant zero-current transition mode.

The zero detection circuit uses displacement current of a sense capacitor C_{ZCD} as shown in typical application. At the inductor current ramps down to zero, the drain voltage of MOSFET begins oscillation. As soon as the ZCD pin voltage falls down to 100mV (V_{ZCDTH}), the MAP3514D initiates next switch cycle.

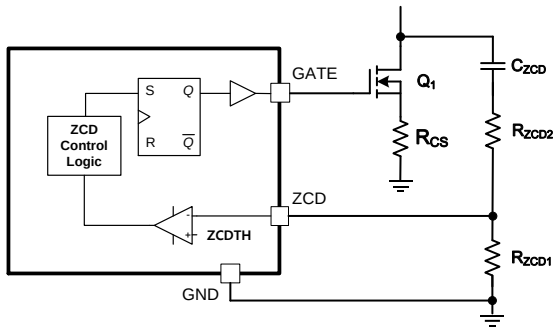


Figure 8. Configuration of analog dimming and current sensing

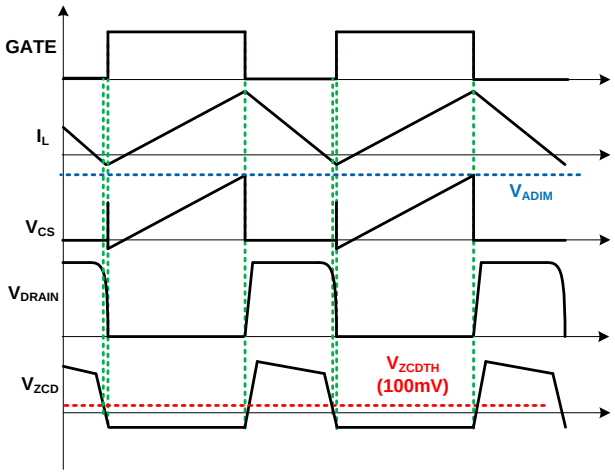


Figure 9. Zero-Current Sense

After MOSFET turned-off, if the ZCD pin voltage keeps less than typ. 100mV (V_{ZCDTH}) for more than typ. 25us ($t_{ZCDTOUT}$), the IC begins next switch cycle forcibly

To prevent abnormal MOSFET turn-on by ZCD, ZCD voltage is masked for 440ns after a MOSFET is turned off internally.

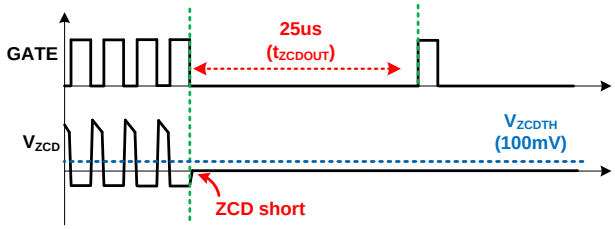


Figure 10. Zero-Current Sense Time Out

PWM DIMMING

The brightness control of the LEDs is performed by a pulse-width modulation. The GATE output is valid only at PWM on period. This means that the GATE maintains off-state as long as PWM signal is logic low.

Care should be taken to test at low PWM duty-cycle because the output capacitor can affect rising and falling time of LED current due to its charging and discharging time.

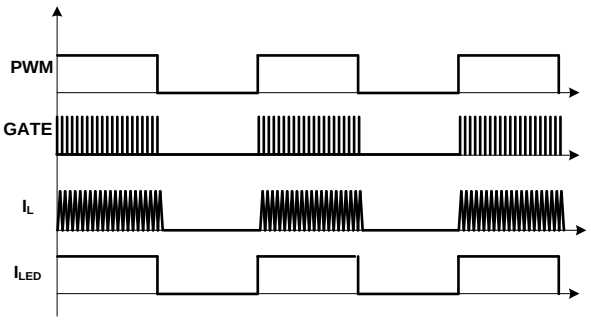


Figure 11. PWM Dimming

STANDBY MODE

The MAP3514D has a standby mode to reduce the power consumption. If the PWM signal keeps a low level for more than typ. 120ms, the MAP3514D turns-off the GATE output and goes on the standby mode. During the standby mode, if the PWM signal is high, the IC wakes up and turns-on the GATE output after typ. 60us.

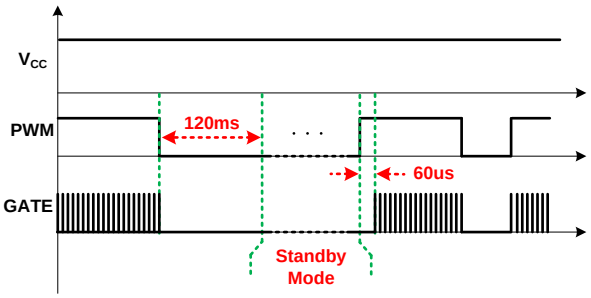


Figure 12. Standby Mode

V_{CC} UNDER VOLTAGE LOCKOUT (UVLO)

The MAP3514D has an Internal LDO regulator to supply internal circuit and GATE driver. This LDO is powered up when the V_{CC} voltage rises to UVLO release threshold.

If the voltage on the V_{CC} pin falls below UVLO lockout threshold, the device turns-off the GATE output and be reset. This ensures fail-safe operation for V_{CC} input voltage falling.

SOFT-START

The MAP3514D operates at peak current mode at initial start-up to smooth inductor current ramp-up

(output capacitor charging phase). The number of peak-controlled switch cycles is 15 times at initial start-up.

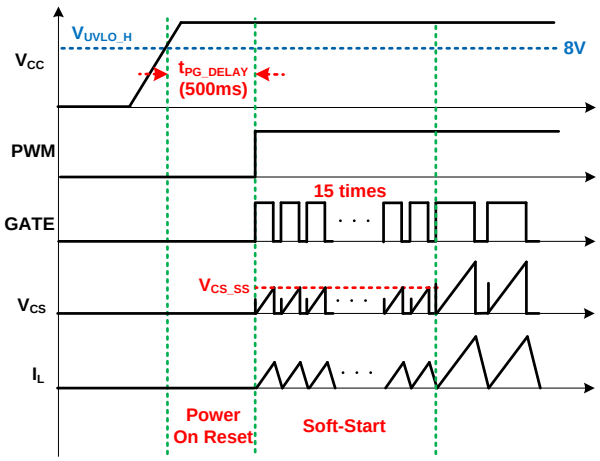


Figure 13. Soft-Stat and UVLO (V_{CC} Rising)

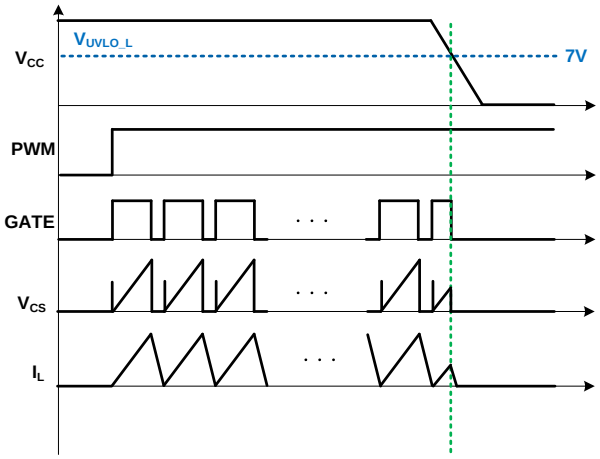


Figure 14. UVLO (V_{CC} Falling)

FLT OUTPUT

FLT pin is an open-drain type output pin. If any of following events occurs, the FLT pin goes to logic Low state immediately. The protection status is latched and can be cleared by applying a complete power-on-reset (POR).

- MOSFET Drain-Source Short Detection
- V_{CC} Over Voltage Protection (OVP)

MOSFET DRAIN-SOURCE SHORT DETECTION

Regardless of PWM logic state, if the CS voltage exceeds V_{SCPDS} for more than typ. 5us (t_{SCPDS}) due to drain-source short of external MOSFET, the FLT pin goes to logic Low state immediately and the GATE output is turned off.

CASE (1) - At PWM Logic High :
If the CS voltage exceeds typ. 2.5V (V_{SCPDS}) for more than 5us, the MOSFET drain-source short protection is occurred.

CASE (2) - At PWM Logic Low :
If the CS voltage exceeds typ. 0.7V (V_{SCPDS}) for more than 5us, the MOSFET drain-source short protection is occurred.

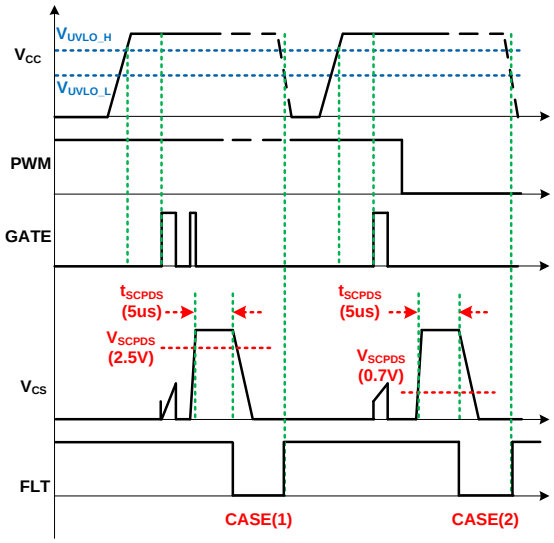


Figure 15. MOSFET Drina-Source Short Detection

V_{CC} OVER VOLTAGE PROTECTION (OVP)

If the V_{CC} voltage exceeds typ. 16V (V_{OVP_VCC}), the FLT pin goes to the logic Low state immediately and the GATE output is turned off. Under the V_{CC} OVP condition, the internal auto-restart signal occurs with 1ms period. When the V_{CC} is less than 16V, the GATE output is turned on by the auto-restart signal. The V_{CC} OVP function does not latch.

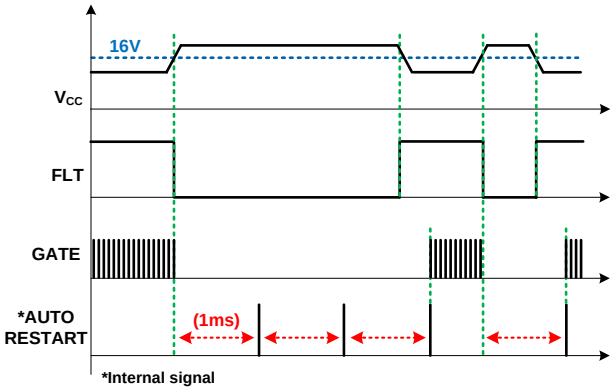


Figure 16. V_{CC} Over Voltage Protection

SHORT CIRCUIT PROTECTION (SCP)

If the CS voltage rises 2.5V (V_{SCP}) during normal operation, the MAP3514D turns-off the GATE output after typ. 300ns (t_{DELAY}). The auto-restart time is typ. 1ms ($t_{RESTART}$). This protects for hard instantaneous short such as free-wheeling diode, inductor or LED bar short.

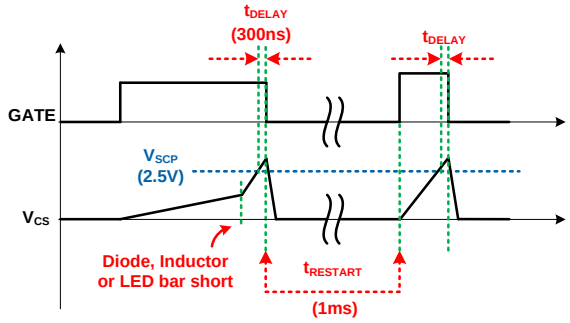


Figure 17. Short Circuit Protection

R_{CS} SHORT PROTECTION

If the CS pin is shorted to GND due to current sense resistor (R_{CS}) short, there is a potential danger of the over-current condition not being detected. The MAP3514D can protect this short event.

If the CS pin voltage is equal or lower than typ. 0.2V (V_{CSP}) for more than typ. 5us (t_{CSP}), the IC turns off the GATE output immediately.

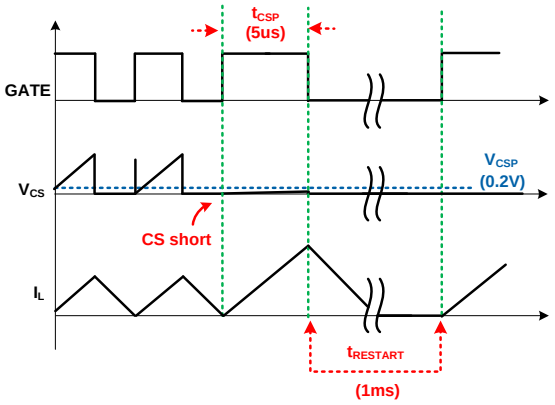


Figure 18. R_{CS} Short Protection

INPUT VOLTAGE PROTECTION

MAP3514D has a LINE pin to detect the input voltage of the QR buck converter. By using the voltage divider to connect the LINE pin, the input voltage is detected and the under/over voltage level of the input voltage can be decided.

- V_{IN} Under Voltage Protection (UVP)
- V_{IN} Over Voltage Protection (OVP)

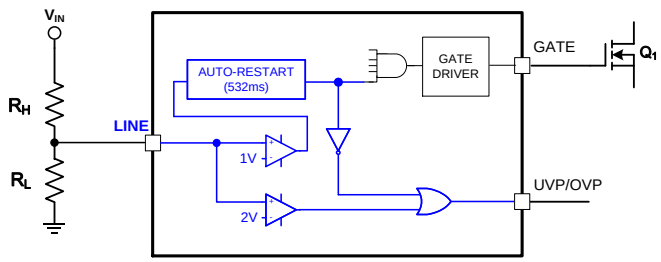


Figure 19. Input Voltage Protection

V_{IN} UNDER VOLTAGE PROTECTION (UVP)

If the LINE voltage is less than typ. 1V for more than typ. 1.5us ($t_{UVP\ LINE}$). The GATE output is turned off, immediately and the high signal (typ. 5V) outputs from the UVP/OVP pin. Under the V_{IN} UVP condition, the internal auto-restart signal occurs with 532ms period. When the LINE voltage is more than typ. 1V, 1.5us ($t_{UVP\ LINE}$) and the internal auto-restart signal is high, the UVP/OVP output is high and the GATE output is turned off, immediately.

The input voltage UVP level, V_{IN_UVP} is decided as follows:

$$V_{IN\_UVP} = 1 \times \frac{R_H + R_L}{R_L} \ [V] \qquad (2)$$

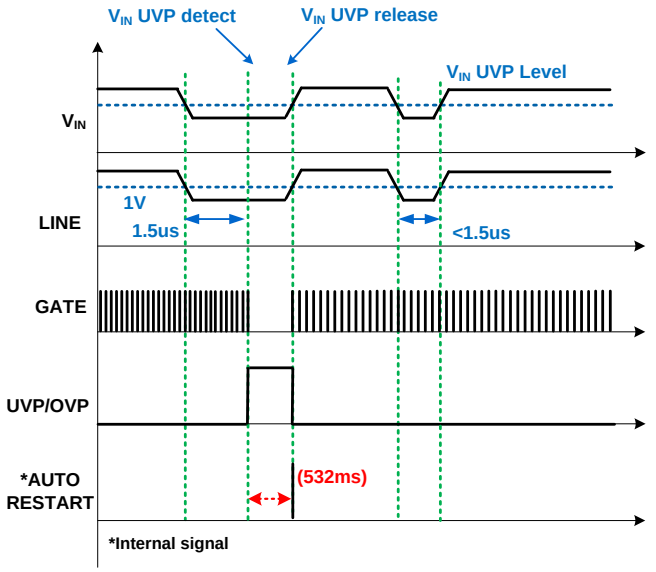


Figure 20. V_{IN} Under Voltage Protection (UVP)

V_{IN} OVER VOLTAGE PROTECTION (OVP)

If the LINE voltage is exceeds than typ. 2V, the high signal (typ. 5V) outputs from the UVP/OVP pin. When the LINE voltage is less than typ. 2V, the UVP/OVP output is Low.

The input voltage OVP level, V_{IN_OVP} is decided as follows:

$$V_{IN\_OVP} = 2 \times V_{IN\_UVP} \ [V] \qquad (3)$$

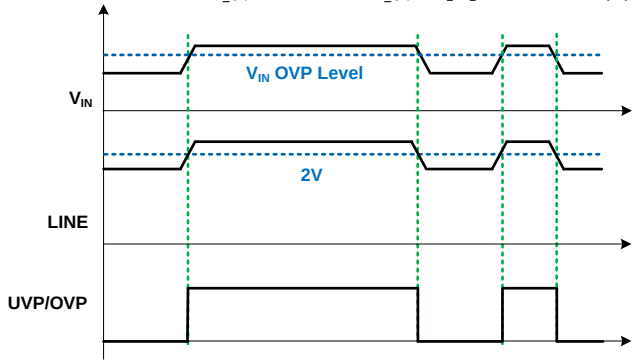


Figure 21. V_{IN} Over Voltage Protection (OVP)

Application Information

LED Backlight Application

In display devices such as TV, monitor, the LED backlight unit is commonly needed for the light source. Figure 22 shows the typical LCD TV system configuration. In the SMPS board, the power factor correction (PFC) module provides high power factor and converts the AC input voltage to the DC link voltage and the isolated DC-DC module provides the regulated DC voltage with galvanic isolation.

In LED backlight panel, as the current through the LED bars increases, the brightness also increases. Therefore, the constant current should be supplied to achieve high-quality light. However, the isolated DC-DC module cannot provide constant current. Hence, the DC-DC LED driver is required to control the constant LED current.

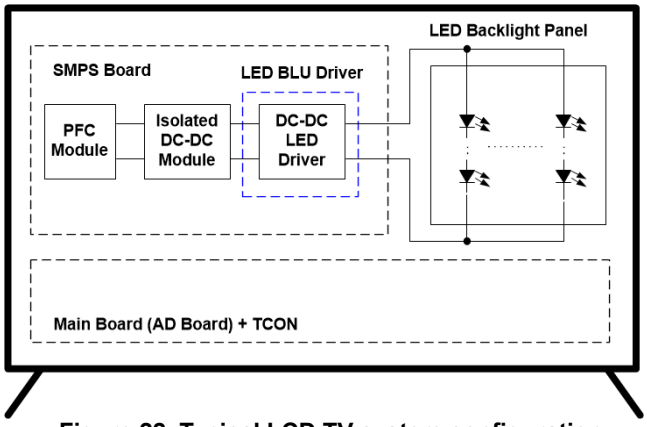


Figure 22. Typical LCD TV system configuration

Buck Converter Topology

The buck converter is known as the step-down DC-DC converter, which converts the input voltage to be lower. Figure 23 shows the circuit diagram of the conventional buck converter. In the conventional buck converter, there is a high-side switch (a floating switch) so the floating gate driver is required.

In order to simplify the control without the floating gate driver, the low-side switch buck converter has been proposed as shown in Figure 24. It is also called a floating buck converter because the output load is floating from the ground. Since the LED load do not require to connect to the ground, this topology can be adopted for LED drivers.

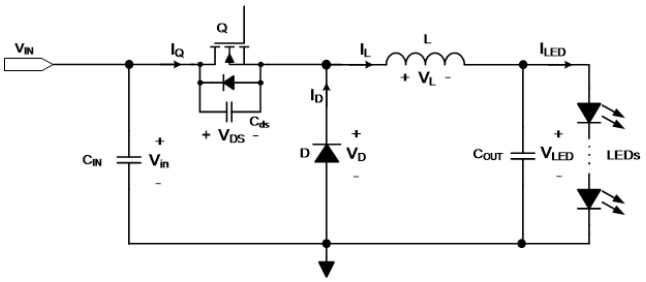


Figure 23. Conventional buck converter

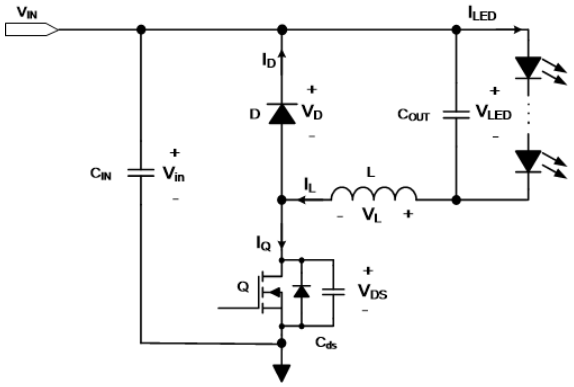


Figure 24. Low-side switch buck converter (Floating Buck converter)

Quasi-Resonant Mode

In order to operate the critical conduction mode (CRM) mode, the quasi-resonant (QR) mode is adopted as the control method. It is known as variable frequency control or valley switching control. Figure 25 shows the principle of the quasi-resonant mode at the low-side switch buck converter. In the discontinuous conduction mode (DCM) operation mode, when the stored energy of the inductor is fully discharged and the inductor current is zero, the resonance between the buck inductor L and the drain-source capacitance C_{ds} of the MOSFET Q occurs. The MOSFET drain-source voltage V_{DS} oscillates as a damped sinusoidal wave. The resonant frequency by the L and C_{ds} is expressed as follows:

$$f_R = \frac{1}{2\pi\sqrt{L \cdot C_{ds}}} \quad (4)$$

In the QR mode, the above-mentioned resonance is used as shown in Figure 25. If the MOSFET is turned on when V_{DS} reaches zero (or low) (which is called valley point), the buck converter is operated in the CRM mode. Because the voltage and current of the MOSFET are zero (or low) at the moment that the MOSFET is turned on, the switching losses are significantly reduced.

In the QR mode operation, the switching frequency f_{SW} is changed according to the input voltage V_{in} and the output power P_{out}. Figure 26 shows the graph of the switching frequency according to the input voltage V_{in} and the output power P_{out}. As the Pout increases, the f_{SW} decreases because longer charging time (on-time) is required to store more energy at the inductor. On the other hand, as the V_{in} increases, the f_{SW} decreases because the same amount of energy can be stored within shorter charging time due to higher V_{in}.

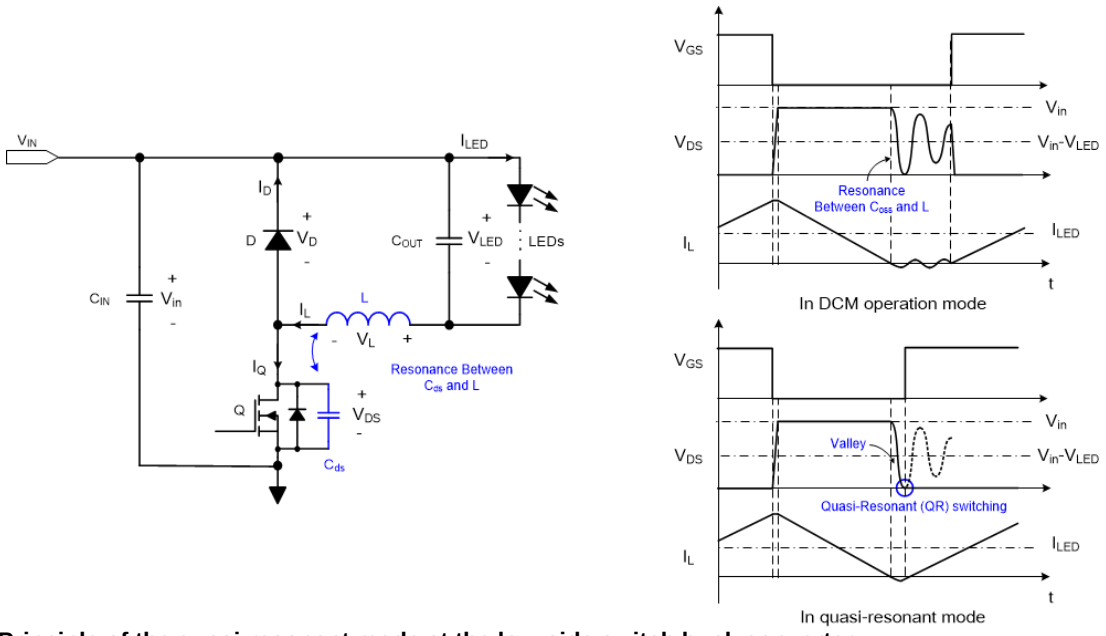


Figure 25. Principle of the quasi-resonant mode at the low-side switch buck converter

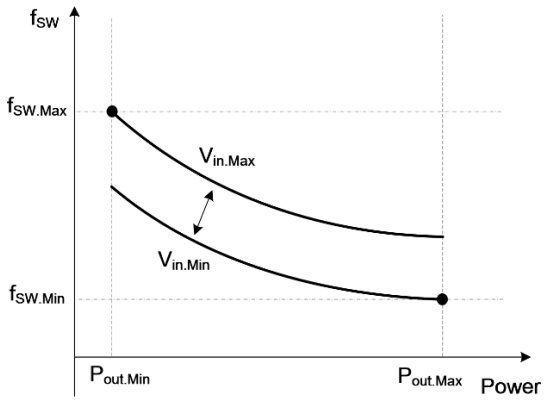


Figure 26. Switching frequency according to V_{in} and P_{out}

Design Guide

1. Input Voltage and LED Voltage Setting

The input voltage is should be higher than the output voltage (the LED voltage) on the buck converter.

$$V_{in} > V_{LED} \quad (5)$$

The voltage of the LED bar is expressed as follows:

$$V_{LED} = V_F \times n \quad (6)$$

Where V_F is the voltage drop of a LED and *n* is the number of LEDs in the LED bar.

2. R_{CS} Selection

In the condition where R_{REF}=R_{ADIM} and V_{ADIM}=3.3V, from (1), the current sensing resistor R_{CS} is calculated as follows:

$$R_{CS} = \frac{0.5V_{ADIM}}{I_{LED.max}} = \frac{0.5 \times (0.66 + 0.3 \times 3.3V)}{I_{LED.max}} \quad (7)$$

From (7), the minimum LED current is obtained as follows:

$$I_{LED.min} = \frac{0.5 \times (0.66 + 0.3 \times 0V)}{R_{CS}} \quad (8)$$

Where V_{ADIM}=0V.

3. Inductance Calculation

If the ideal CRM Buck converter as shown in Fig. 27, the ideal on-time is calculated as follows:

$$t_{on\_ideal} = \frac{V_{LED}}{V_{in} f_{sw}} \quad (9)$$

In the Ideal CRM Buck converter, the peak inductor current $I_{L.pk}$ is twice the LED current I_{LED}. From (9), the ideal inductance of L is calculated as follows:

$$L_{ideal} = \frac{V_{in} - V_{LED}}{I_{L.pk}} t_{on\_ideal} \quad (10)$$

4. Quasi-Resonant Time

In the QR Buck converter, the turn-on delay time t_{delay} is existed by the resonance between C_{ds} and L. Unfortunately, it is impossible to calculate the actual quasi-resonant time. The most of the parasitic capacitances affecting the resonance are unknown except the output capacitance C_{oss} of the MOSFET.

In order to operate close to CRM operation mode, the t_{delay} must be very small enough with minimal design impact. In the design example, C_{ds} was considered as 100pF.

From (4), the turn-on delay time t_{delay} is calculated as follows:

$$t_{delay} \approx \pi \sqrt{L \cdot C_{ds}}/2 \quad (11)$$

However, the calculated t_{delay} is not correct because the C_{ds} is not real value and the t_{delay} can be changed by the ZCD detection timing (the turn-on timing).

We recommend using the measured t_{delay} for the converter design.

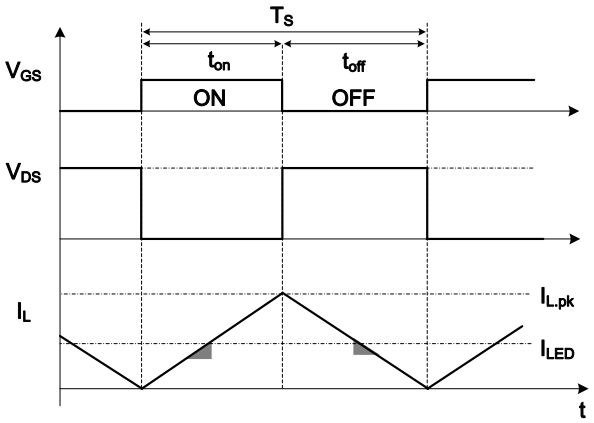


Figure 27. Key waveforms of the Ideal CRM Buck converter

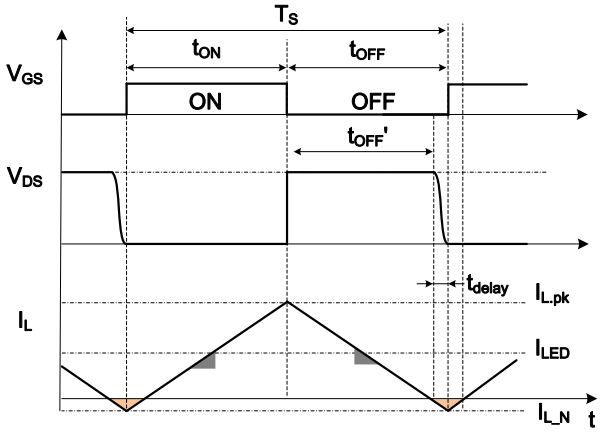


Figure 28. Key waveforms of the QR Buck converter

5. Inductor Current

By the turn-on delay time t_{delay}, the inductor current decreases to negative. Therefore, the inductor peak current $I_{L.pk}$ is slightly higher than the twice of the LED current I_{LED}.

The negative inductor current I_{L_N} is estimated as follows:

$$I_{L\_N} \approx -\frac{V_{LED}}{L} t_{delay} \quad (12)$$

However, the calculated I_{L_N} is not correct because the I_{L_N} decreases nonlinearly by the resonant.

We recommend using the measured I_{L_N} for the converter design.

From (10), the peak inductor current $I_{L.pk}$ is estimated as follows:

$$I_{L.pk} \approx 2I_{LED.max} - I_{L\_N} \quad (13)$$

6. Switching Frequency

In the QR Buck converter, by the turn-on delay time t_{delay}, the switching frequency f_{SW} is less than the target switching.

$$f_{SW} < f_{SW\_target} \quad (14)$$

During a single-switching period, the switching period T_s is expressed as follows:

$$T_s = t_{ON} + t_{OFF} = t_{ON} + t_{OFF}' + t_{delay} \quad (15)$$

The on-time t_{on} is obtained as follows:

$$t_{ON} = (I_{L.pk} - I_{L\_N}) \frac{L}{V_{in} - V_{LED}} \quad (16)$$

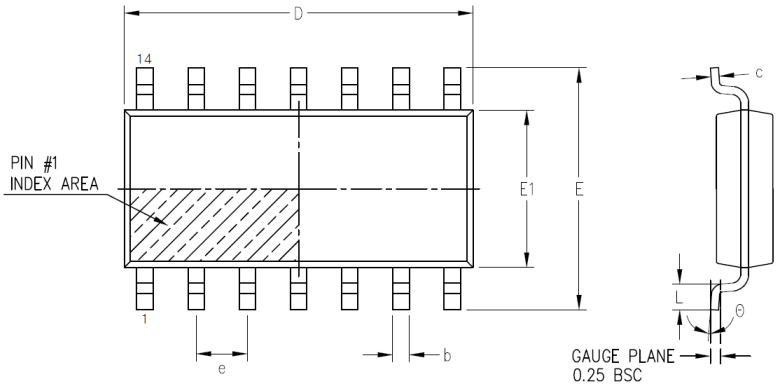
The discharging time t_{OFF}' is obtained as follows:

$$t_{OFF}' = I_{L.pk} \frac{L}{V_{LED}} \quad (17)$$

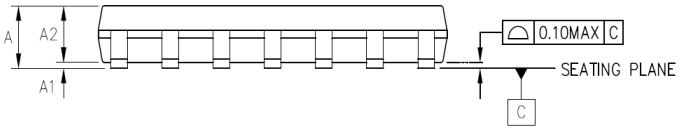
From (11), (15), (16) and (17) the switching frequency is obtained as follows:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}' + t_{delay}} \quad (18)$$

Physical Dimensions



Symbol	Dimension (mm)		
	Min	Nom	Max
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	–	1.27
θ	0°	–	8°



NOTES :

1. Reference JEDEC MS-012(AB)
2. Package length and width do not include mold flash, protrusions or gate burrs.
3. The configuration of PIN #1 identifier/chamfer feature is optional

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